A Fully Integrated 5.9GHz RF Frontend in 0.25um GaN-on-SiC for Vehicle-to-Vehicle Applications

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Abstract — This paper presents the design of a high-efficiency and high-power RF frontend for the 802.11p standard, leveraging an embedded Tx/Rx switching scheme and a dual-bias power amplifier (PA) linearization technique. The fully integrated RF frontend is fabricated in 0.25um GaN-on-SiC technology and occupies 2mm x 1.2mm. In the Tx mode, the PA+Tx switch achieves 48.5% drain efficiency at 33.9dBm Psat with 28V supply. With OFDM-modulated signals, it achieves 30% average efficiency at 27.8dBm output power while meeting the 25dB EVM limit without predistortion. In the Rx mode, the LNA+Rx switch achieves +22dBm OIP3 with 8dB power gain at 12V supply. The fully integrated high-efficiency and linear RF frontend is demonstrated at high output power for vehicular communications for the first time.

Index Terms — RF frontend, GaN, power amplifiers, LNAs, antenna switches, and IEEE 802.11p

I. INTRODUCTION

The emergent IEEE 802.11p-based dedicated short range communication (DSRC) standard [1] is customized for vehicular environments. To communicate with other cars on the road at up to 1km range, the maximum allowed output power is 28.8dBm at 5.9GHz frequency band with the same OFDM-based modulation as the IEEE 802.11a standard. However, CMOS circuits have not been able to achieve such high output power at 5GHz while maintaining linearity or good error vector magnitude (EVM) even though much effort was put into increasing the efficiency and output power of a CMOS linear power amplifier (PA) for 5GHz wireless local area network (WLAN) applications [2].

It is well known that GaN devices outperform CMOS devices for PAs in terms of output power and efficiency. Since automobiles represent an energy-constrained environment, we leverage GaN for a high-power and high-efficiency PA design for IEEE 802.11p applications. At the same time, a linear GaN-based low noise amplifier (LNA) can be employed in RF frontends since the receiver is also required to be highly linear to accommodate input signals with minimum sensitivity along with potential high-power interferers from nearby 802.11p transmitters. Due to the high power handling capability, small on-resistance and high isolation characteristics of the GaN devices, on-chip antenna switches can also be taken into account for high level of integration of RF frontends including a PA, an LNA, and Tx/Rx antenna switches on a single die, which enables the reduction of packaging cost and system form factor since high-power RF frontends have traditionally relied on multi-chip modules or discrete designs.

In addition, the fully integrated RF frontend can benefit from both architectural and circuit-level techniques to further improve efficiency. In this paper, a new Tx/Rx switching scheme and a dual-bias linearization technique are proposed to enhance system energy efficiency.

II. RF FRONTEND ARCHITECTURE

An explicit antenna switch is usually employed in both the Tx and Rx branches in order to switch modes in a time division duplex (TDD) radio, as shown in Fig. 1(a). The Tx branch switch exhibits high insertion loss around 1dB at 5.9GHz [3] in addition to consuming significant additional die area, impacting overall Tx performance. If the PA produces an output power of P_{OUT,PA}, and the Tx switch has a loss of P_{L,TXSW}, then the achievable Tx output power at the antenna port is:
\[ P_{\text{OUT}} = P_{\text{OUT,PA}} - P_{L,TXSW} \]

Similarly, if the PA efficiency is given by \( \eta_{PA} \), then the overall Tx efficiency is:

\[ \eta = \eta_{PA} \times 10^{-\left(\frac{P_{L,TXSW}}{10}\right)} \]

For example, assuming that a single-pole-double-through (SPDT) switch with 1dB loss is added to 1W (=30dBm) PA with 50% drain efficiency, the overall Tx power and efficiency is 794.3mW (=29dBm) and 39.7%, respectively. Thus, Tx branch switch loss has a dramatic impact on overall Tx performance.

Fig. 1(b) shows the proposed architecture, focusing on co-design of the Tx and Rx paths to essentially eliminate the Tx branch switch for efficiency enhancement. No explicit switch is included in the Tx branch. Instead, the drain of the PA transistor is directly connected to the Rx section.

In the Tx mode, the PA output matching network presents the optimum impedance \( Z_L \) (when loaded by a 50Ω antenna), extracting maximum power from the GaN power transistors. Under this condition, the drain of the PA device sees large voltage swings up to 2\( V_{DD} \). The series-shunt switch in the Rx branch isolates and protects the inactive LNA from this voltage stress. In the RX mode, the PA transistors are turned off with a sufficiently low gate bias and isolated from the PA input by employing the PA input switch which is off, providing a small but finite capacitance \( C_{O,PA} \) at the drain node. Thus, the LNA input should be simply matched to the parallel combination of \( Z_L \) and \( C_{O,PA} \) to maximize power gain and minimize noise figure.

### III. CIRCUIT DESIGN

#### A. PA + Switch design

For the design of a high-efficiency 802.11p compliant PA the high peak-to-average power ratio (PAPR) of complex modulated signals should be considered to satisfy the linearity requirement simultaneously. In this work, a Class-C device with its input and output combined in phase with a Class-AB device [4] is adopted without additional tail devices for higher efficiency and more compact integration of the RF frontend.

Fig. 2 shows the simulated individual transconductances, \( G_{m1}/G_{m2} \) for Class-AB/C over a range of drive voltages, as well as the linearized composite transconductance, \( G_m \). Since Class-AB amplifiers have to be backed-off from their 1dB point to meet system linearity and/or EVM requirements, a low \( P_{1dB} \) point corresponds to lower average efficiency. However, with help of the combined Class-C device, the \( P_{1dB} \) point of the PA increases through cancellation of the compressive nonlinearity, enhancing the average efficiency.

The PA is optimized through large-signal load-pull simulation, specifying impedance vectors up to the third harmonics. Initially, the source impedance is set to \( Z_0 \) to determine \( Z_L \) with load-pull, and then a source-pull is performed to find \( Z_S \). Since efficiency is more sensitive to load impedance, the optimal \( Z_L \) is used, while a somewhat non-optimal \( Z_S \) is chosen in order to improve stability. Small on-resistance of the PA input switch in the Tx mode, shown in Fig. 1, acts as a series stabilization resistance, absorbing the switch loss.

The complete PA schematic is depicted in Fig. 3 with the corresponding component values. At the drain, the shunt-L series-C provides impedance matching from \( Z_0 \) to \( Z_L \), DC bias and RF signal coupling with only two elements. A series-C shunt-L is chosen for the gate as it performs the transformation from \( Z_0 \) to \( Z_S \) and splits the RF signal into the two gates in phase for the dual-bias Class-AB + Class-C topology.

#### B. LNA + Switch design

In this proposed RF frontend architecture, the Rx switch is directly connected to the drain of the PA, as shown in Fig. 4(a). In the Tx mode, the LNA input, \( V_{LNA} \), is grounded through \( M_{\text{SHUNT}} \) and the voltage stress is shared equally in the divider formed by the parasitic capacitors \( C_p \) of \( M_{\text{SERIES}} \), which is off. The control voltage \( V_{\text{OFF}} \) should be chosen...
such that the RF voltage stress does not accidentally turn on $M_{\text{SERIES}}$. Using the process parameters with the maximum expected $V_{\text{DD}}$, $V_{\text{OFF}} = -25$ V was found to provide adequate margin for this design because the depletion mode GaN device has the negative threshold voltage. The switch is sized to keep loss under 0.5 dB and provides about 30 dB of isolation which is more than adequate to protect the LNA.

In the Rx mode, the LNA needs a reactive input impedance $Z_{\text{LNA}}$ which forms the conjugate power match with $Z_{\text{TX}}$ and the Rx switch. The Rx switch is simply a small series resistance, $R_{\text{ON}}$, therefore the matching condition is:

$$Z_{\text{RX}}(\omega) = \text{Re}(Z_{\text{LNA}}(\omega)) + R_{\text{ON}} + \text{Im}(Z_{\text{LNA}}(\omega)) = Z_{\text{TX}}(\omega)^*$$

It is well known that inductively degenerated LNAs are capable of synthesizing a reactive input match with independent control of real and imaginary parts. Fig. 4(b) shows the complete LNA schematic with the corresponding component values.

IV. IMPLEMENTATION

A prototype based on the proposed architecture was designed in Cree 0.25um GaN-on-SiC technology. The die micrograph is shown in Fig. 5. Total die area is 2.0 mm x 1.2 mm including the RF frontend circuits with passive matching and biasing components, as well as decoupling capacitors. Spiral inductors built with a single thick metal layer and high-voltage metal-insulator-metal capacitors are used to design all matching networks. The process also offers through-wafer-vias, which were used extensively for low-inductance grounding. Co-simulation with foundry supplied device models and EM simulation-based models is conducted for final verification of the design and layout.

For good thermal and electrical performance, a combination of eutectic die attachment followed by chip-on-board (COB) technology is selected. The PCB is designed on a high dielectric constant, low-loss Rogers-3010 material. To minimize the wire bonding effects at 5.9 GHz, on-chip decoupling capacitors are integrated for both PA and LNA supplies and multiple bonding wires are used for RF input and output ports.

V. MEASUREMENTS

Fig. 6(a) shows the small-signal response of the RF frontend in the Tx mode, with the Rx port terminated. S11 is better than -20 dB while S21 is around 10 dB for the band of interest (i.e. 5.850 GHz - 5.925 GHz). The small-signal response of the Rx mode is shown in Fig. 6(b). S11 is better than -13 dB while S21 is around 8 dB. Noise figure (NF) is measured with a calibrated noise source and found to be 3.7 - 4.0 dB in band. Since the LNA active device is not downsized aggressively to maintain correlation with device models which are not fitted to very small geometries, it partially affects LNA performance. Tx-Rx path isolation (not shown here) is better than -45 dB in band.
Fig. 7. (a) Dual-bias linearization, (b) Tx power sweep

Fig. 8. (a) Tx performance with OFDM, (b) EVM with 20MHz bandwidth OFDM signal at 5.875 GHz

Fig. 9. Output third-order intercept of the LNA

VI. CONCLUSION

This paper demonstrates a fully integrated, high-power and high-efficiency RF frontend for the 802.11p standard. By employing a newly proposed switching scheme and a dual-bias linearization technique, both high efficiency and linearity are achieved. The RF frontend is fabricated using 0.25um GaN-on-SiC process and is the first single-chip RF frontend for vehicular applications at 5.9 GHz.

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