Physical vs. Virtual Express Topologies with Low-Swing Links for Future Many-core NoCs

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***Abstract*—The number of cores present on-chip is increasing rapidly. The on-chip network that connects these cores needs to scale efficiently. The topology of on-chip networks is an important design choice that affects how these networks scale. Most current on-chip networks use 2-D mesh topologies which do not scale due to their large diameter and energy inefficiency. To tackle the scalability problem of 2-D meshes, various physical express topologies and virtual express topologies have been proposed. In addition, recently proposed link designs like capacitively driven low-swing interconnects can help lower link power and latency, and can favor these bypass designs. In this work, we compare these two kinds of express topologies under realistic system constraints using synthetic network traffic. We observe that both express topologies help reduce low-load latencies. Virtual topologies help improve throughput whereas the physical express topologies give better performance-per-watt.**

I. Introduction

With Moore's law providing more and more transistors on-chip, architects have embraced many-core architectures to deal with increasing design complexity and power consumption of conventional single-processor chips. There are already fabricated designs with 10s of cores on a single chip [9], [17]. Going forward, we could have 100s or even 1000s of cores on a single die. These many-core architectures employ many simpler cores and interconnect the cores using a scalable on-chip network fabric. To meet the bandwidth demands of these cores, designers use packet-switched on-chip interconnection networks and have moved beyond conventional shared buses.

Selecting an appropriate topology is one of the most critical decisions in the design of on-chip networks; it impacts the zero-load latency and sustainable bandwidth, and also influences the power consumption of the network. Most existing on-chip networks utilize a 2-D mesh topology [6], [9], [17], as meshes have lower design complexity and map well to the 2-D chip substrate. However, they are energy inefficient because the high network diameter leads to extra router hops to reach the destination, and router energy is high relative to link energy [9]. This poses serious scalability concerns for such topologies as node count increases in the future. To tackle the scalability issues of 2-D mesh, various express topologies have been proposed in the literature. One set of proposals employ long physical links between non-local routers to reduce the effective network diameter [4], [7], [12]. We will refer to these topologies as *physical express topologies.* Another set of proposals use various techniques to opportunistically bypass router pipelines at intermediate network hops and thus save on network latency and power [14]–[16]. We will refer to these techniques as *virtual express topologies.*

Both physical and virtual express topologies have their advantages and disadvantages. Physical express topologies reduce the network diameter, thereby saving the latency and power due to bypassing of intermediate router hops. To accomplish the physical bypass paths, however, extra router ports, larger crossbars and extra physical channels are required. Extra router ports and larger crossbars lead to higher router area and power. While on-chip wires are relatively abundant, use of large number of dedicated point-to-point links leads to a large area footprint and low channel utilization. Virtual express topologies have the advantage that they do not use extra long physical links. However, the bypass of routers in such designs is opportunistic and not guaranteed. The virtual router bypass also differs from physical bypass in that the bypassing flits still have to multiplex through the router crossbar and output link, while in a physical bypass, all intermediate routers and links are bypassed completely.

The long links in the physical express topologies can also leverage some of the recent innovative low-swing interconnect proposals. Specifically, capacitively driven low-swing interconnects (CDLSI) [8] have the potential to save significant energy while also providing modest latency reductions. CDLSI links can be used as single-cycle multi-hop express links that provide further latency savings since long hops can be covered in a single cycle and the power consumption would also be less, owing to the low-swing nature of these links. The low power of the CDLSI links can also be exploited by all the topologies for connecting neighboring routers.

Although there are clear trade-offs between various physical and virtual express topologies, to the best of our knowledge, there has been no work comparing these various topology alternatives for many-core network on-chips (NoCs). In this paper, we compare a particular physical express topology (express physical channels (EPC) based on express cubes [4]), to a virtual express topology proposal (express virtual channels (EVC) [14]) for large node count on-chip networks. We present energy, area, latency and throughput results for a 256

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node configuration with synthetic network traffic. We observe that both EPC and EVC help in lowering low-load latency. However, while the EVC network is more robust across traffic patterns, and offers a higher throughput than baseline for most cases, the EPC network is more traffic dependent and bisection bandwidth dependent. If we compare the performance-per-watt, however, EPC with CDLSI links turns out to be the best.

The main contributions of this work are as follows.

- We present a detailed characterization of how CDLSI links could be leveraged for long and short hop links to be used in various express topologies.
- We present a detailed comparison of physical and virtual express topologies for large node-count systems under different design constraints (bisection bandwidth, router area, and power).

The rest of the paper is organized as follows. Section II provides circuit level details of CDLSI links and its latency, area, and energy properties. Section III discusses various physical and virtual express topologies proposed in the literature and motivates the need for comparison amongst them. Section IV discusses the evaluation methodology and presents quantitative results, and Section V concludes.

II. Capacitively Driven Low-Swing Interconnects

Conventional low-swing interconnects are attractive to NoC designs as they reduce the power consumption by reducing the voltage swing on the wires [18]. But this advantage is usually accompanied by a penalty in latency. Moreover, they usually require a second voltage power supply.

Capacitively Driven Low-Swing Interconnects (CDLSI) were proposed by Ho. et al. in [8]. The design involves driving wires through a series capacitor, and these interconnects have been shown to have excellent energy savings without the degradation of performance. The use of the coupling capacitor results in a low-swing wire without the need for a second power supply. It also extends the wire bandwidth by introducing pre-emphasizing effects and significantly reduces the driver energy consumption.

The differential and twisted wires enable the signals to be sent at a low voltage swing, and eliminate the coupling noise. But this comes at the cost of 2X wiring area. The link area model we used in our experiments can be formulated as $A_{Cu} = (2w_{flit} - 1)lw$ for normal non-differential Cu wires and $A_{CDLSI} = (4w_{flit} - 1)lw$ for CDLSI wires, where A_{Cu} stands for the area of a conventional Cu wire, A_{CDLSI} stands for the area of a CDLSI wire, w_{flit} is the flit-width, l is the link length, and w is both the width of the link and the spacing between two wires. The spacing between the links is assumed to be the same as the link-width.

We applied a delay-power optimization, which is similar to the approach in [11], to both normal Cu wires and CDLSI wires. Detailed analysis of this approach can be found in [13]. For normal Cu wires, more than half of the total power is consumed by the wire. On the other hand, for CDLSI wires, transceivers consume most of the power. As a result, for a given delay penalty, the impact on power saving in CDLSI wires is greater than that in normal Cu wires.

	length	$1mm$		$2mm$		$4mm$	
	BW	D(ps)	E(fJ)	D(ps)	E(fJ)	D(ps)	E(fJ)
CDLSI	1Gbps	108	22.4	215	27	430	61
	2Gbps	108	22.4	215	27	430	61
	3Gbps	108	22.4	194	30.4	430	61
	4Gbps	101	27.3	175	35.8	368	71.5
	5Gbps	94	35.2	162	43.6	330	87.2
Normal	1-10Gbps	108	133	215	265	430	531

TABLE I
Delay(D) and energy(E) consumption of CDLSI wire and normal Cu wire for different lengths and bandwidths

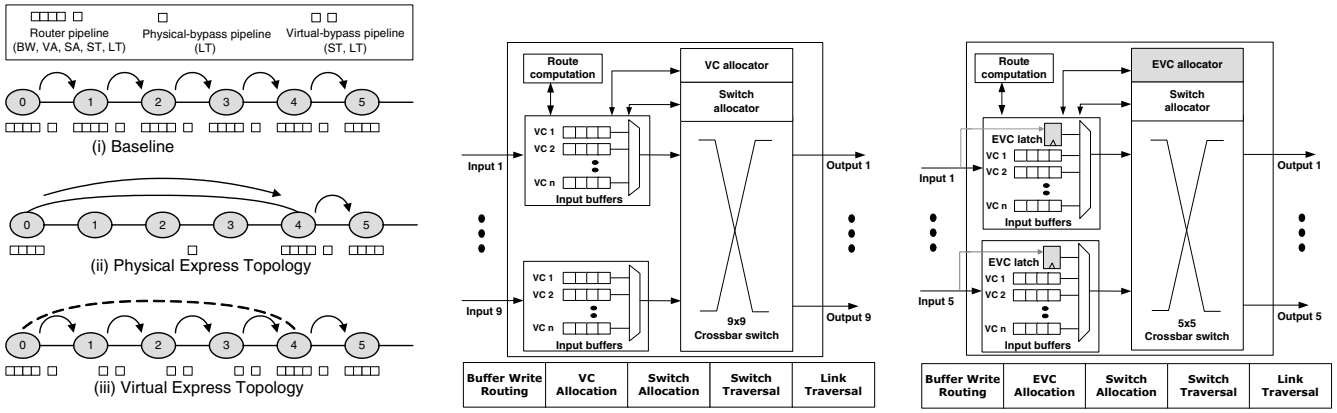
Table I shows the latency and energy consumption of a CDLSI wire as a function of different wire lengths and bandwidths with 192 nm wire width at 32 nm technology node. The wire width and the wire spacing are chosen to be four times the minimum wire width defined in ITRS [1] to meet the bandwidth requirements in our experiments. The table also shows the numbers for normal Cu wires. The energy consumption of a CDLSI wire is approximately 10x less than that of a normal Cu wire with the same wire length and bandwidth below 3 Gbps. It should be noted that CDLSI wires consume ultra-low energy even as the length of the wire increases. This property enables the use of CDLSI wires as express links for multi-hop communication. For example, the delay for a 4mm long CDLSI wire is 330 ps, that is, it is within two cycles for a 5GHz clock frequency, whereas the it takes three cycles to traverse a normal Cu wire of the same length.

III. Express Topologies

An ideal interconnection network between processing cores in CMPs would be point-to-point, where the latency of the messages is equal to just the link latency, and there are no additional penalties due to contention and corresponding arbitration. However, such a network is not scalable, requiring $N - 1$ links per node in a N node network, which will blow up the area footprint. This has led to researchers proposing packet-switched networks with intermediate routers to multiplex the available bandwidth [3]. The router microarchitecture for such a network is described next.

A. Baseline Router

A NoC router typically has a 5-stage pipeline [5], with four stages in the router, and one in the link. In the first stage, the incoming flit gets buffered (BW-Buffer Write), and performs routing for determining the output port to go out from. In the second stage (VA-VC Allocation), the flits at all input ports arbitrate for virtual channels (VCs) at the next router. In the third stage (SA-Switch Allocation), the flits at all input ports, which have been assigned output VCs, now arbitrate for using the crossbar that will connect this input port to the required output port. In the fourth stage (ST-Switch Traversal), the flits that won the switch traverse the crossbar. Finally, in the fifth stage (LT-Link Traversal), flits coming out of the switch traverse the link till the next router. A packet can go through VA and SA multiple times depending on the contention, until it

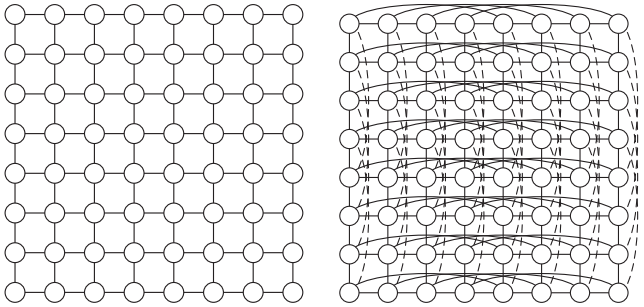


(a) Comparison of the path taken by a flit going from router 0 to router 5 in the Baseline, Physical Express Topologies, and Virtual Express Topologies

(b) EPC Router Microarchitecture

(c) EVC Router Microarchitecture

Fig. 1. Comparison of Express Topologies



(a) 8x8 Baseline and EVC network

(b) 8x8 EPC network

Fig. 2. Network topology

succeeds in obtaining a VC and switch. Thus each flit entering a router takes multiple cycles before it can make a hop to the next router. This design will be referred to as the *baseline* design in the rest of the paper.

This solution of having hop-by-hop traversal through multiple intermediate routers is simple and effective. However, spending multiple arbitration cycles in intermediate routers would add unnecessary delay to packets traveling longer distances, especially in future many core chips. Moreover, the buffering and arbitrations at the routers add to the power consumed. Thus, there have been many proposals that advocate for packets traveling longer distances to *bypass* intermediate routers. We characterize these into two categories.

- *physical express topologies:* adding physical channels to skip intermediate routers.
- *virtual express topologies:* having means to bypass arbitration and buffering at the intermediate routers.

The basic ideas behind these techniques are shown in Figure 1(a), and described next.

B. Physical Express Topologies

Physical express topologies argue for physical express links between far away routers. Non-local packets can traverse these express links (i.e. LT) to avoid getting delayed at intermediate routers, and also not add to contention at the ports there. Moreover, this eliminates the power that these packets would consume at the intermediate routers. The trade-off however is that each router now needs to have multiple ports, which in turn requires a bigger crossbar. The area and power of a crossbar increase as a square of the number of ports times the link width, and thus more ports is a potential concern. Moreover, the available metal area on-chip could add a limitation on the number of express links that can be added. Reducing the link width can address some of these concerns, but that would add serialization latency to the packets.

Express Cubes [4], Flattened Butterfly [12] and MECS [7] are examples of physical express topologies. Express Cubes was a proposal for the multi-chassis shared-memory multiprocessor (SMP) domain for connecting nodes that are multiple hops away to reduce latency. Flattened butterfly is an on-chip network topology that uses routers with high port counts to map a richly connected butterfly network onto a two-dimensional substrate using a two-level hierarchy. It reduces the network diameter to two, thus minimizing the impact of multiple router hops. However, the total number of links required in each dimension grows quadratically with the number of nodes in the dimension. Multi-drop express channels (MECS) [7] uses a one-to-many communication model enabling a high degree of connectivity in a bandwidth efficient manner. It solves flattened butterfly's problem of requiring too many links by using an express multi-drop bus originating from each router to connect other routers along the dimension. However, the crossbar has only one port per direction like the baseline, and so all the express links entering a router from a particular direction need to multiplex on the same crossbar port, thereby sacrificing throughput.

C. Virtual Express Topologies

Virtual Express Topologies are a class of flow-control and router microarchitecture designs that reduce router energy/delay overheads by creating dynamic fast paths in a network. The basic idea is that flits try to bypass buffering and arbitrations at the router, and proceed straight to the switch (ST) and link traversals (LT), thereby reducing the latency,

and power (as buffer reads/writes and VC/Switch arbitrations are skipped). The flits that fail to bypass get buffered and proceed through the conventional baseline pipeline described in Section III-A. No extra physical links are required, and the crossbar is same as the baseline crossbar. However, this means that the incoming flits from various ports (which wish to bypass the router), and the locally buffered flits, all need to multiplex on the same output links. Virtual express topology proposals essentially describe efficient ways of performing this multiplexing, such that most flits are able to bypass the routers along their path.

Express Virtual Channels (EVC) [14], Token Flow Control (TFC) [15] and Prediction Router [16] are examples of virtual express topology proposals. Express Virtual Channels statically partitions all the VCs into 1-hop, 2-hop, ... l_{max}-hop *express* VCs (EVCs). Flits arbitrate for appropriate EVCs during VA depending on their route. A flit that gets a k-hop EVC can bypass the k-1 intermediate routers along that dimension, by sending a lookahead one cycle in advance to preallocate the crossbar at the next router. EVCs use deterministic XY routing, and do not allow bypassing at turns, to avoid contention among different lookaheads. Token Flow Control also enables router bypassing by obtaining and chaining together *tokens* (hints about buffers and VCs at neighboring routers) to form arbitrarily long bypass paths. It supports contention among lookaheads, thereby allowing adaptive routing, and bypassing along turns. Prediction Router [16] enables bypassing by predicting the output port and setting up the switch a-priori.

D. Chosen Topologies

We choose a 16x16 mesh as our baseline topology, Due to limited space, a smaller 8x8 mesh example is shown in Figure 2(a), with each router having 5-ports, and implementing the 5-stage pipeline described in Section III-A. The physical express topology we use for our evaluation studies is based on express cubes and uses 9-port routers, with express links connecting each router to the router that is 4-hops away, in each direction, as shown in Figure 2(b). We refer to this topology as *Express Physical Channels (EPC)*.

The virtual express topology we use for our experiments is EVC, since it maps well to the EPC design by not allowing turning paths, and restricting the bypassing to a maximum of l_{max} hops (which we choose to be four in our design)[1] at a time. The EVC topology uses a 16x16 mesh like the baseline.

EPC and EVC might not be the best possible physical and virtual express topologies for all scenarios in their individual domains, but they capture the essential properties of these design spaces that we wish to compare, namely the performance, power and area implications of long physical links and high crossbar ports versus opportunistic bypass and multiplexing on the crossbar ports and links.

Figure 1 shows micro architecture of the EPC and EVC routers.

[1]Higher values of l_{max} complicate flow-control signaling and result in diminishing returns [14]

Technology	32 *nm*
V_{dd}	1.0 V
$V_{threshold}$	0.7 V
Frequency	5 GHz
Topology	16-ary 2-mesh (The physical express topologies have additional express links)
Routing	Dimension ordered X-Y routing
Synthetic Traffic	Uniform Random, Tornado, Bit Complement

TABLE II
SIMULATION PARAMETERS

Fig. 3. Equalized bisection bandwidth.

IV. EVALUATION

In this section, we present a detailed comparison of a physical express topology, Express Physical Channels (EPC), and a virtual express topology, Express Virtual Channels (EVC), using both conventional full-swing copper interconnects and CDLSI low-swing links. We study the configurations along three dimensions under which future NoCs might be constrained, namely, bisection bandwidth, chip area and power. The simulation infrastructure and the various experiments are described next.

A. Simulation Infrastructure

To compare the different configurations, we used a cycle-level on-chip network simulator, GARNET [2]. GARNET models a detailed 5-stage router pipeline as described in Section III. We used ORION 2.0 [10], an architecture-level network energy and area model, to evaluate the power consumption and area footprint of routers. For the links, we use the numbers discussed in Section II. All our experiments were done at 32nm technology node. In our results, we report only dynamic power and not leakage power. This is because at 32 nm technology node, leakage power is expected to be pretty high and aggressive leakage reduction techniques would be employed to reduce overall power consumption. Such techniques are not modeled in ORION, and thus we choose not to report leakage power. Evaluation with synthetic traffic uses packets which uniformly consist of either 8-byte control packets or 72-byte data packets. We assume three message classes out of which two always carry control packets and one is dedicated to data packets. This was done to closely match modern cache coherence protocol requirements, as was done in [14]. Table II lists various network parameters that are common to all the configurations we evaluated for synthetic traffic. We ran experiments for uniform random, tornado and bit complement traffic. We do not report results for tornado traffic since the trends were very similar to uniform random traffic. Next, we describe various topology configurations that we evaluated.

B. Configurations

We evaluate two sets of configurations across all topologies. First we assume normal Cu wires for the links. We then perform experiments using CDLSI links for both local and express links in all topologies.

1) Configurations with normal Cu wires: For the EPC topology, we assume 1mm links between routers, and 4mm express links. It takes three cycles to traverse these express 4mm paths, as discussed in Section II. For the EVC network, it is assumed that the EVC flits spend one cycle traversing the router (ST), and one cycle traversing the links (LT). The reverse signaling for buffer and VC flow-control is assumed to take one cycle for both EPC and EVC. The baseline design is the 5-stage router design described in Section III.

Future NoC designs could be constrained along different dimensions depending on system requirements. Three constraints which we feel NoC designs might face are bisection bandwidth, chip area and power consumption. With this in mind, we perform experiments to compare the various topologies under the above constraints. After fixing a constraint, we perform design-space explorations to find out the best performing configuration for the particular topology. For the baseline design, we assume 128-bit links (flit-width). Varying the flit-width of the baseline will change the parameters of other topologies when we normalize designs. To study it's effect, we performed all our experiments with varying baseline flit-width and found that the conclusions of our experiments do not change. Hence we report results with 128-bit flit-width as baseline. We will refer to this configuration as *Baseline*. With 128-bit flit-width, a 72-byte data packet has five flits, while an 8-byte control packet forms one flit.

As mentioned before, we perform three sets of experiments: one in which bisection bandwidth across designs is equalized, another in which the router area is equalized and finally we compare designs given the same power budget.

Configuration with equalized bisection bandwidth: In the first set of experiments, we keep the bisection bandwidth across all topologies constant. The EVC topology has the same number of ports at the *Baseline* topology and hence the flit-width remains the same as 128 bits. As with every configuration we choose the number of buffers and VCs that leads to the best performance for the EVC topology. We call this configuration *EVC-bw*. The EPC topology has five times as many channels at the bisection cut of the *Baseline* design. To equalize the bisection bandwidth, the flit-width of the EPC design thus becomes one-fifth of that of the baseline, which is 24 bits. This is shown in Figure 3. A 72-byte data packet thus consists of 24 flits, whereas an 8-byte control packet is composed of three flits. Now we vary the number of VCs and buffers and find out the best performing configuration. This will be called *EPC-bw* in the rest of the paper.

Configuration with equalized router area: In the second experiment, we equalize the router area across all configurations. The crossbar and buffers are the major area consuming components in a router and hence we equalize them. The parameters of the router that impact crossbar and buffer area are flit-width, number of VCs and number of buffers. We sweep the design space for the EPC and EVC topologies, varying the above three parameters so that the total area is same as that of *Baseline*. We report results for the best performing configurations and call them *EVC-area* and *EPC-area*.

	Flit width (bit)	#VC/msg class	#Buffer/port
Baseline	128	6	36
Baseline-CDLSI	128	6	36
EVC-bw	128	12	84
EVC-area	128	6	36
EPC-bw	24	4	108
EPC-area	64	6	66
EVC-bw-CDLSI	128	12	84
EVC-area-CDLSI	128	6	36
EPC-bw-CDLSI	24	4	108
EPC-area-CDLSI	64	6	66

TABLE III
TOPOLOGY PARAMETERS

Configuration with same power budget: We plot the power-performance curve for all the designs and configurations that we studied and compare the performance of the designs under the same power budget. We did not have to run additional configurations for this study.

2) Configurations with CDLSI wires: We also evaluate all the topologies using CDLSI wires instead of conventional wires, and all other parameters remaining the same as before. We again assume 1mm links between routers, and 4mm express links. It takes 2 cycles to traverse these express paths using CDLSI wires. The configurations are called *Baseline-CDLSI, EVC-bw-CDLSI, EVC-area-CDLSI, EPC-bw-CDLSI,* and *EPC-area-CDLSI*. Table III shows all the configurations.

C. Results

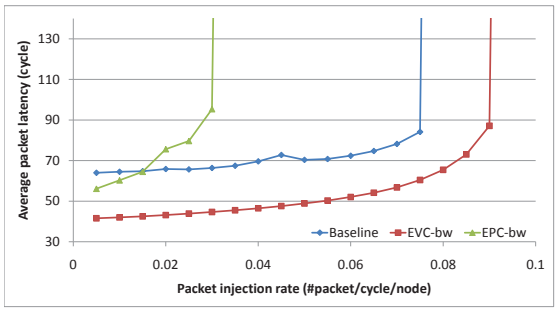
We evaluate the above mentioned configurations with a 16x16 mesh topology. We first present the performance results for the various studies.

1) Normal Cu wires: The results with normal Cu wires are presented next.

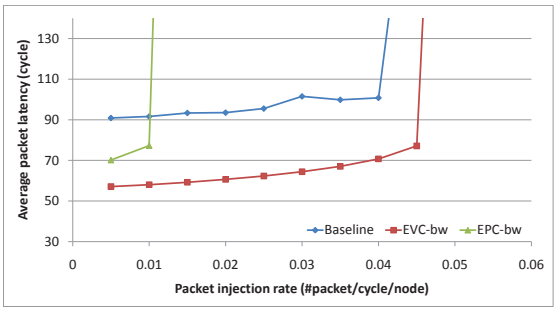
Same bisection bandwidth: Figure 4 shows the relative performance (packet latency vs. injection throughput) of various topologies for different synthetic traffic, given the same bisection bandwidth. Note, we do not show tornado traffic as it had results similar to uniform random traffic.

For both uniform random and bit complement traffic, we observe that *Baseline* has the highest latency at low loads. The *EPC-bw* has the second highest latency and *EVC-bw* has the lowest low-load latency. The high hop-count of the baseline network leads to extra router and link hops resulting in higher low-load latencies. Both *EVC-bw* and *EPC-bw* bypass intermediate router pipelines and thus have lower low load latencies. The maximum difference in low-load latencies is for the bit complement traffic. This is because in bit complement traffic, the source and destinations are farthest away, leading to the best utilization of express paths (both virtual and physical).

Although, *EPC-bw* completely bypasses the routers and *EVC-bw* bypasses only certain pipeline stages, the low-load latency for *EVC-bw* is lower. This is because of very low flit-widths in the *EPC-bw* networks. The *EVC-bw* network has a flit-width of 128 bits and equalizing the bisection bandwidth results in the *EPC-bw* network having a flit-width of 24 bits. A data packet (72 bytes) thus has 24 flits for *EPC-bw*, and 6 flits for *EVC-bw*. The higher serialization latency of the physical express topology far outweighs the benefits of

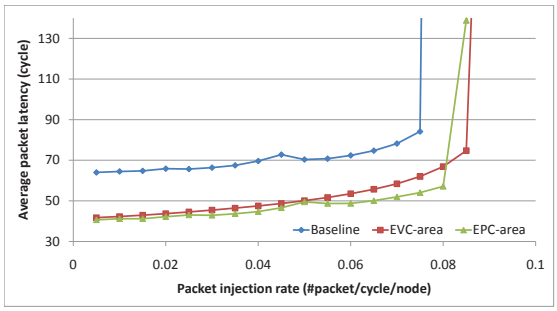


(a) Uniform Random Traffic

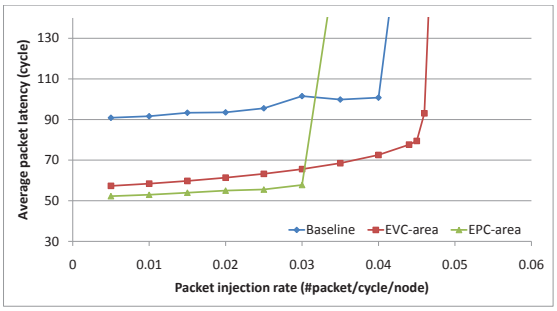


(b) Bit Complement Traffic

Fig. 4. Network performance of various topologies with normal Cu wires under same bisection bandwidth



(a) Uniform Random Traffic



(b) Bit Complement Traffic

Fig. 5. Network performance of various topologies with normal Cu wires under same router area

complete physical bypasses, leading to overall higher latency than *EVC-bw*.

In terms of throughput, the *Baseline* and the *EVC-bw* have much better saturation throughput than *EPC-bw* for all traffic patterns. This is because physical express topologies do not optimally utilize the available link bandwidth. *EVC-bw* outperforms *Baseline* due to router bypasses and pushes the saturation throughput towards the ideal.

In summary, given the same bisection bandwidth, *EPC-bw* performs worse than *EVC-bw* due to serialization effects and poor bandwidth utilization.

Similar router area: Figure 5 shows the relative performance (packet latency vs. injection throughput) of various topologies for different synthetic traffic patterns, given the same router area budget. When comparing topologies, with the router area normalized, we observe that the *Baseline* has the highest latency at low loads. The *EPC-area* network has the lowest low-load latency for both traffic patterns, although it is only marginally better than *EVC-area* for uniform random traffic. Unlike the equalized bisection bandwidth case, (where *EPC-bw* loses out to *EVC-bw* due to higher serialization latency), the 64-bit *EPC-area* topology has lower serialization latencies leading to better low-load latencies.

In terms of throughput, *EVC-area* and *EPC-area* have better throughput than *Baseline* for uniform random traffic due to better utilization of resources and lesser contention. *EPC-area*, however loses out on throughput to *EVC-area* because the partitioning of links leads to poorer utilization of physical links. For bit complement traffic, the throughput of *EPC-area*

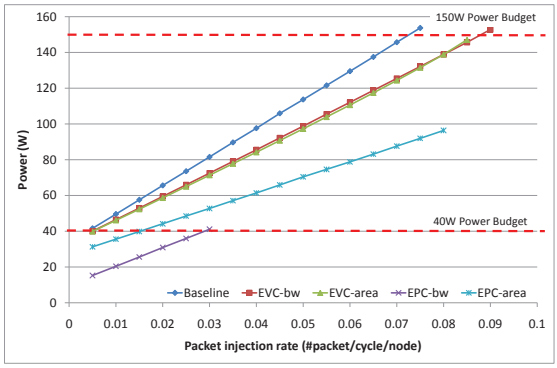


Fig. 6. Power-Performance Curve with Normal Cu Wires

is even worse than that of the *Baseline*. Our implementation of EPC networks assumes static routing and if a packet wishes to use an express link, it keeps on trying for it even if the local links are idle. In bit complement traffic, most of the traffic goes across the chip and thus requires express links. The static nature of our routing therefore leads to poorer utilization of local links and hence the inferior throughput. Smarter adaptive routing algorithms are required to choose between the local and express links for such express topologies and that is beyond the scope of this study.

In summary, given the same router area budget, the performance of *EPC-area* is highly traffic dependent, while *EVC-area* is more robust.

Similar power budget: Many-core CMPs are already facing the power wall and if we go by current trends, the primary

design constraint that future NoCs will face might be power. An NoC architect might need to choose between a set of network topologies, given a network power constraint. The performance evaluations from the equal bisection bandwidth and equal router area concluded in favor of EVC networks due to higher throughput than EPC and comparable low-load latencies. However, the complete picture can be seen in Figure 6 which shows the network power consumption of all topologies with varying performance for uniform random traffic. Given this plot and a network power budget, one can choose the best performing network topology. For e.g., if the total on-chip network power budget is 40W, the *EPC-bw* network is the best performing one, even though in terms of absolute latency and throughput, it is the worst as seen before. *EPC-bw* has the lowest flit-width amongst all configurations and that leads to lower buffer, crossbar and link power consumption. However, if the desired throughput is higher than the saturation throughput of *EPC-bw*, the network power budget would have to be increased and *EPC-area* becomes a winner now since it is lower power than the EVC networks for the same throughput. But once EPC networks saturate, EVC networks perform the best at higher network budgets like 150W. The *Baseline* network always performs worse than EVC and EPC networks under a given power budget. Note that the observed power consumption of these topologies is much higher than what actual designs would allow in future, but there is a huge body of work that tackles the power consumption of routers and how to minimize that. The discussion of such works are beyond the scope of this work.

In summary, EPC topologies are more attractive than the EVC networks from a performance/watt perspective as long as they meet the desired throughput.

2) CDLSI wires: The results with CDLSI wires are presented next.

Same bisection bandwidth: Figure 7 shows the relative performance (packet latency vs injection throughput) of different topologies with various synthetic traffic and given the same bisection bandwidth. The addition of CDLSI links does not affect the relative trends that were observed in the comparisons without CDLSI links. We thus, do not discuss these results and refer the readers to Section IV-C1.

Similar router area: Figure 8 shows the relative performance (packets injected per cycle) of various topologies for synthetic traffic and given the same router area. Adding CDLSI links to the EPC topology leads to lower long-hop latencies and the 4-hop links now take only two cycles to traverse, whereas it took three cycles with normal Cu wires. Lower long-hop latency speeds up packet delivery and eases contention and thus leads to better overall throughput. The effect of this is seen in the uniform random traffic case, where we see that *EPC-area-CDLSI* has a better throughput than *EVC-area-CDLSI*. The trend was opposite with normal Cu wires. Thus, CDLSI wires help EPC topologies outperform EVC topologies, making them an attractive design under certain scenarios. With bit complement traffic, the relative performance of various topologies is similar to what was seen with normal Cu wires in Section IV-C1.

Similar power budget: CDLSI links do not affect the relative power consumption trends that we observed in Figure 6 with normal Cu links. We thus, do not discuss the details of the observation again.

3) Power breakdown: In order to understand the power consumption of various topologies, we study the power breakdown of various on-chip network components. Figure 9 shows the detailed network power breakdown normalized to the total power consumed by *Baseline*. As expected, the topologies with CDLSI links have lower power as compared to the same topology with Cu wires. This is due to the low-swing nature of CDLSI links. The link power of the CDLSI topologies goes down dramatically, thus lowering the overall power consumption. Another observation is that the buffers, crossbar and clock are the major power consuming components in the router. This is as expected. The EPC networks have the lowest overall power, primarily due to the reduced flit-widths that these networks have. This reduces buffer and crossbar power. Interestingly, lower flit-width also eases the load on the clock distribution network thus lowering clock power in the router. The power consumption of the allocators is negligible.

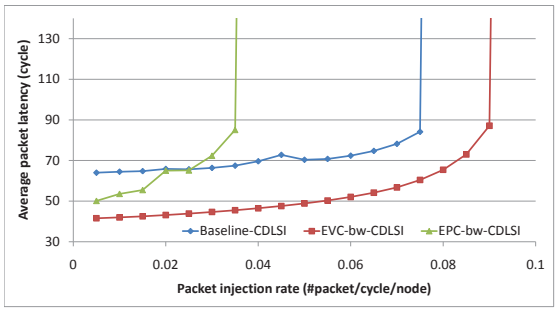
D. Discussion

We summarize the findings of our experiments next.

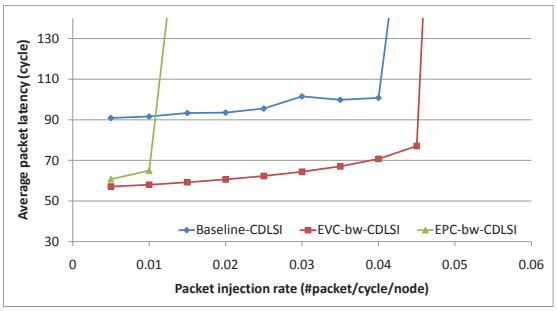
- Virtual express topologies provide the best throughput configuration, given the same resources, and are more robust across all traffic patterns.
- The latency and throughput of physical express topologies degrades a lot with thinner links due to the serialization latency.
- Given sufficient link width (bisection bandwidth), the performance of physical express topologies is highly traffic dependent. While uniform random traffic is able to extract the benefits of the express links and local links, traffic patterns like nearest neighbor would result in complete non-utilization of express links, while bit-complement needs to rely on an adaptive routing scheme to remove contention on the express links.
- When CDLSI links are used, the physical express topologies leverage the low latency physical express links to achieve the best low load latencies and also improve throughput.
- When performance/watt is considered, the physical express topologies are the better choice, until they saturate. After that express virtual topologies seem to perform best for a given power budget.

V. Conclusion

In this paper, we compared the effectiveness of physical and virtual express topologies for meshes with large node counts, under constraints of bisection bandwidth, router area, and power. We also evaluated the impact of the capacitively-driven low-swing interconnect (CDLSI) links on all designs. We observed that while both designs have similar low-load latencies, virtual express topologies give higher throughputs and are more robust across traffic patterns. Physical express topologies, however, deliver a better throughput/watt, and can leverage CDLSI to lower the latency, and increase throughput.

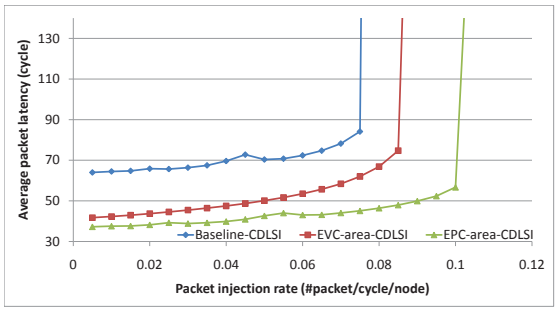


(a) Uniform Random Traffic

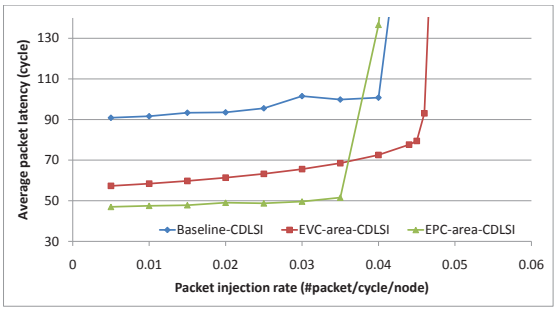


(b) Bit Complement Traffic

Fig. 7. Network performance of various topologies with CDLSI wires under same bisection bandwidth



(a) Uniform Random Traffic



(b) Bit Complement Traffic

Fig. 8. Network performance of various topologies with CDLSI wires under same router area

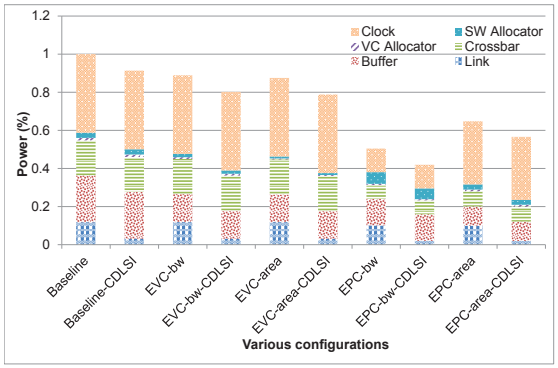


Fig. 9. Network power breakdown for various topologies

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