

1.0 Overview

The Anadigmvortex development board is an easy-to-use platform designed to help you get started with implementing and testing your analog designs on the Anadigmvortex FPAA silicon devices.

While the device on this development platform is an AN221E04 device, you can use this board to implement all of your AN221E02, AN120E04, AN121E04, AN220E04 and AN221E04 designs. The design software - AnadigmDesigner®2 – can use the AN221E04 device on board to implement designs done using any device in the Anadigmvortex device family.

This manual provides an overview on how to effectively use this board to implement your analog design. But first, here are some salient features of the Anadigmvortex development board:

- Small footprint – 4 by 4 inches
- Large breadboard area around the AN221E04 device
- Header pins for all the FPAA device analog I/Os
- Ability to separate, electrically and physically, the digital section leaving a purely analog board with SPI EPROM and digital interface pins
- Four (jumper configurable) analog interface blocks for level-shifting, amplifying, attenuating, filtering and differential to single-ended conversion of the signal
- A spare opamp powered to 5V that can be used to buffer the +0.5V or +3.5V references or an analog signal
- Daisy chain capability – that allows multiple boards to be connected to evaluate multi-chip systems
- Standard PC serial interface for downloading AnadigmDesigner®2 circuit files
- On-board 16-MHz oscillator module

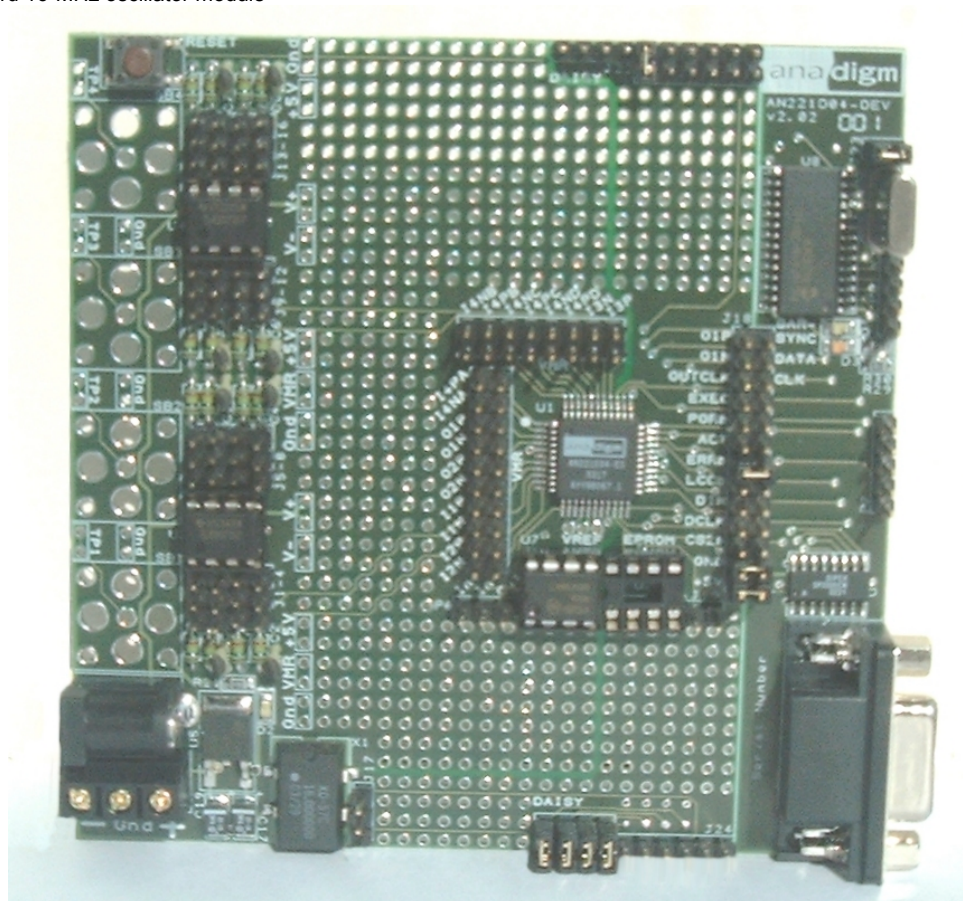


Figure 1: The NEW Anadigmvortex Development Board

2.0 Layout

Figures 2 and 3 show the layout of the board allowing easy location of all the components, power connections and jumpers.

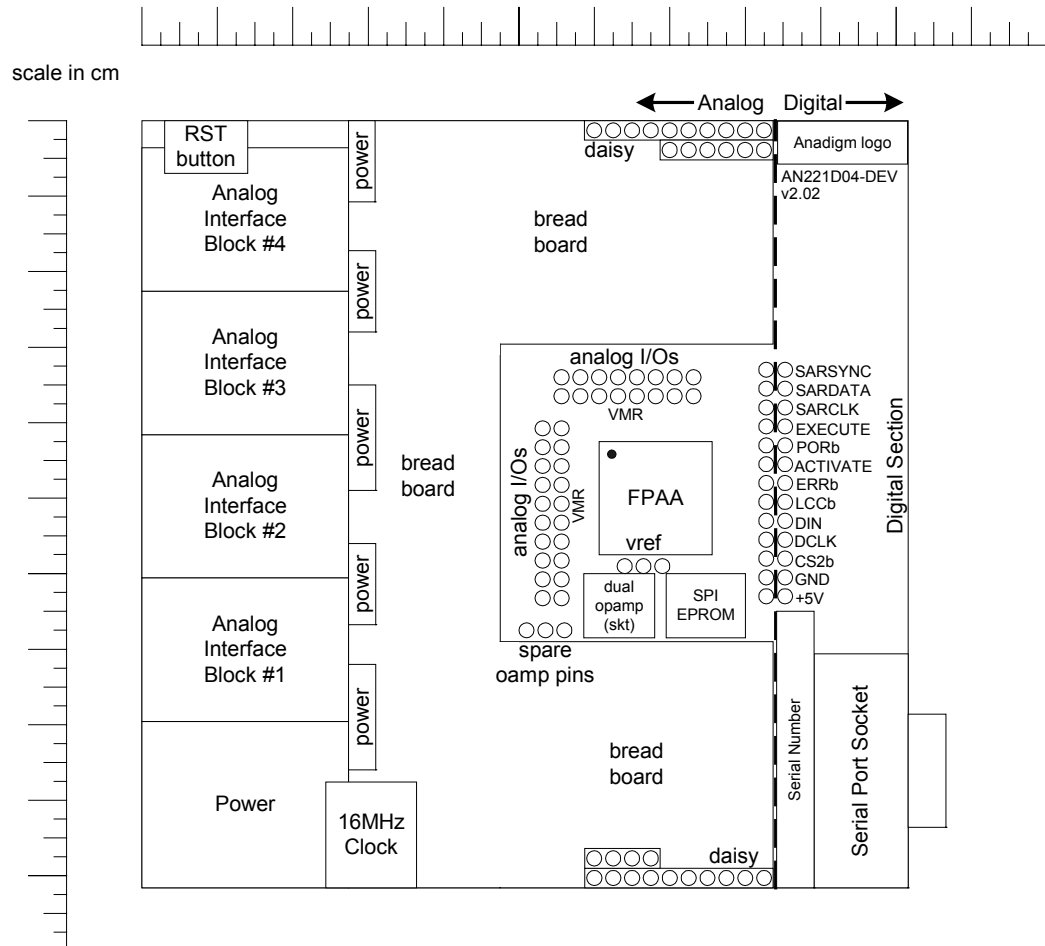


Figure 2: Top-level layout of the Anadigmvortex development board

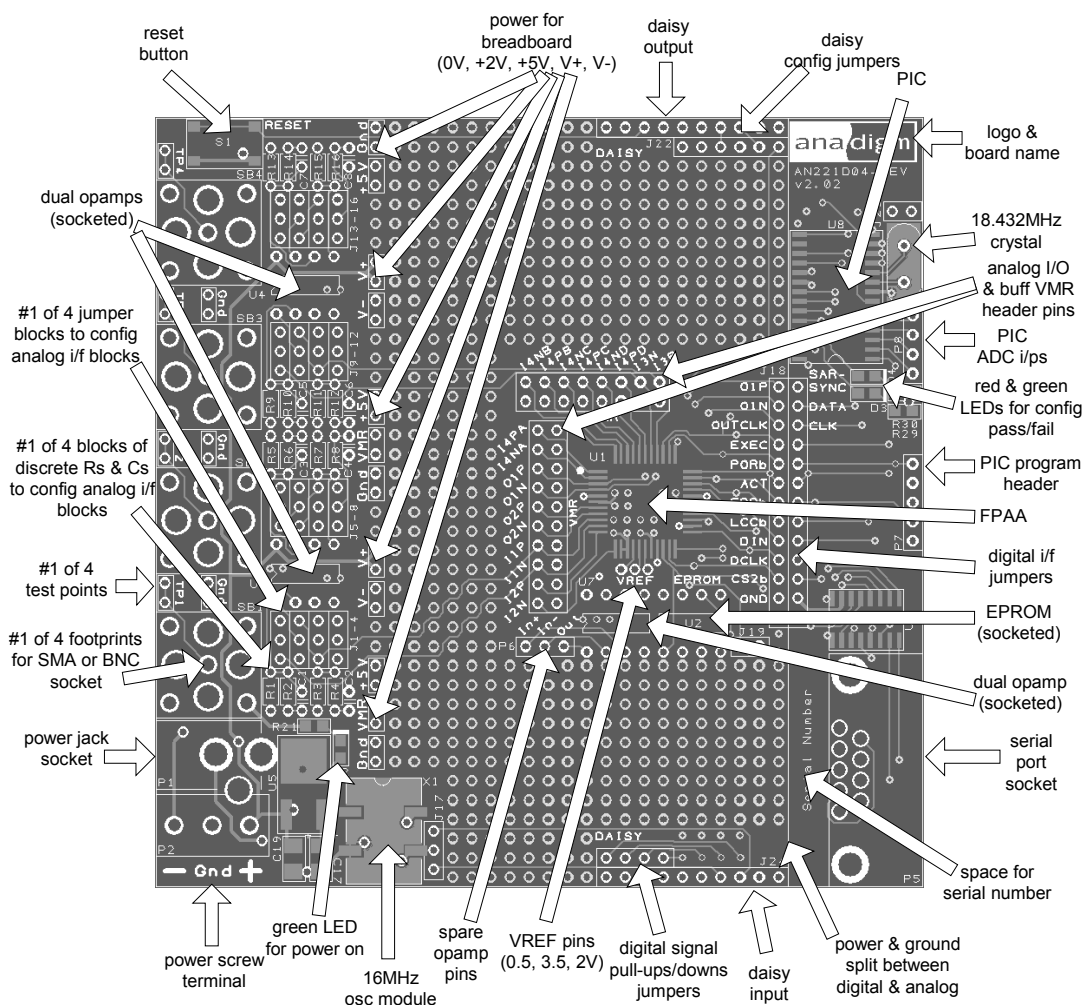


Figure 3: Detailed layout the Anadigmvortex development board

3.0 Powering up the Anadigmvortex Development Board

The options for powering up the board are as follows:

- Connect wire from a dual precision, regulated supply to the on-board 3-way terminal– with negative post at 0V to -10V, middle post at ground, positive post at +5.5V to +10V, OR
- Connect wire from a single precision, regulated supply to the on-board 3-way terminal – with negative post shorted to middle post, +5.5V to +10V across middle and positive posts (cannot use ground referenced signals with analog interface blocks with this mode because $V_- = 0V$), OR
- Use an AC wall converter (regulated) and connect into the supply jack socket, 10.5V minimum, 20V maximum

WARNING

When using an AC wall converter or brick it is important to note the following:

1. The output must be between 10.5V and 20V. A 9V power unit will not work.
2. The output must be regulated if it is intended to use the analog interface blocks.
3. Do not connect the ground post to the negative post of the 3 way screw terminal. This will blow one of the regulators.
4. Be aware that some of the components in the power circuit get hot.
5. When daisy chaining boards, use a single AC converter into one of the boards and common together the negative, ground and positive posts of the screw terminals of all the boards.

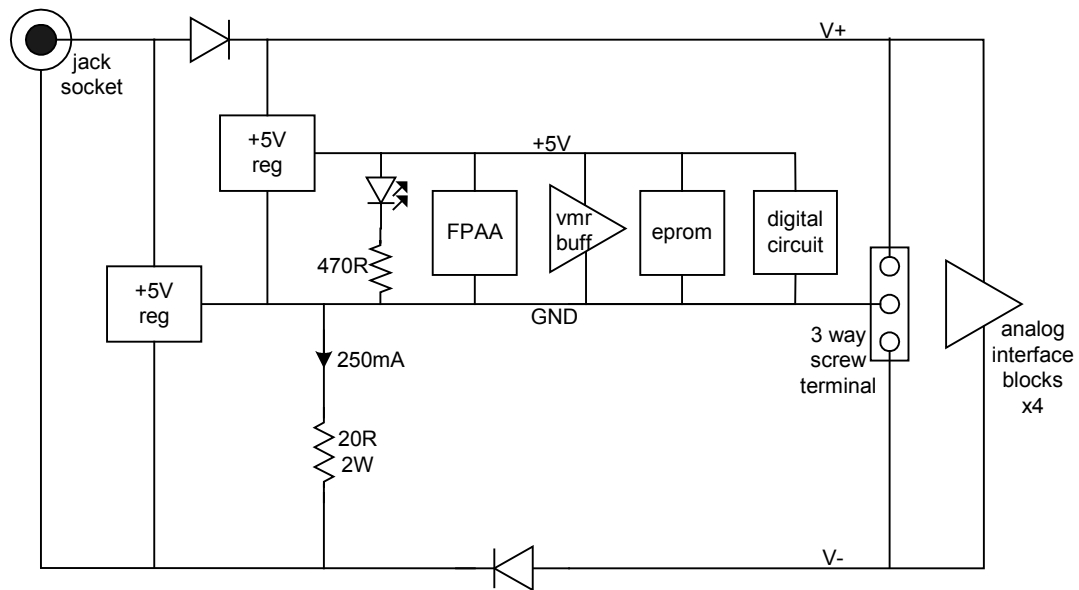


Figure 4: Power Circuit

There is a green LED to indicate that the board is successfully powered up. The current through the FPAA, VMR buffer, EPROM (if used), digital circuitry and anything else connected to the +5V supply on the board is limited to 250mA when using the jack socket power input.

Note: the positive and negative supplies (V+ and V-) determine the amplitude range of signals used with the analog interface blocks.

4.0 Analog Interface Blocks

There are four (4) identical analog interface blocks (figure 5), each with 4 jumpers, a low noise opamp and a set of through-hole resistors and capacitors. These 4 blocks are each connected to an analog input/output pin of the AN221E04 FPAA device. This allows all 4 blocks to be used as either an input or output interface. The 4 blocks are laid out in order up the left side of the board with block #1 at the bottom and block #4 at the top. Each block has a footprint that will take a variety of sockets including SMA and BNC. There is also a test point (TP1-4) and ground point in which the user can solder loops of wire for the connection of probes.

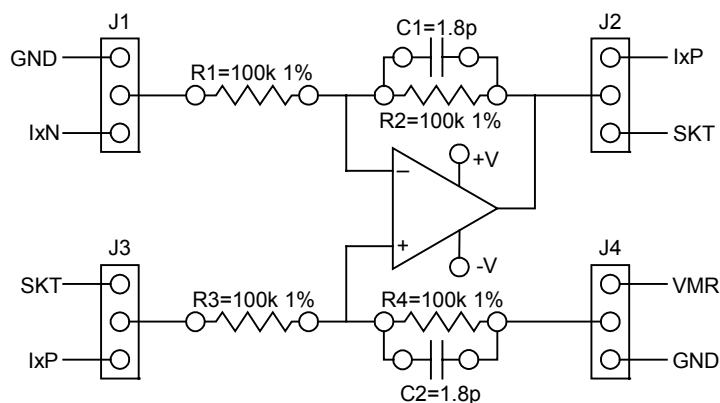


Figure 5: Analog Interface Block (#1 of 4)

If the 4 jumpers are in the upper position then the block is configured as an input stage, level shifting the ground referenced single-ended input to +2V (figure 6). The negative differential input of the FPAA has been shorted to buffered VMR by placing a jumper between its header pin and VMR. The gain of this circuit can be changed by changing the values of the resistors. The gain is given by the following equation:

$$\text{Gain} = R2 / R1 = R4 / R3 \quad - R3 = R1 \text{ and } R4 = R2$$

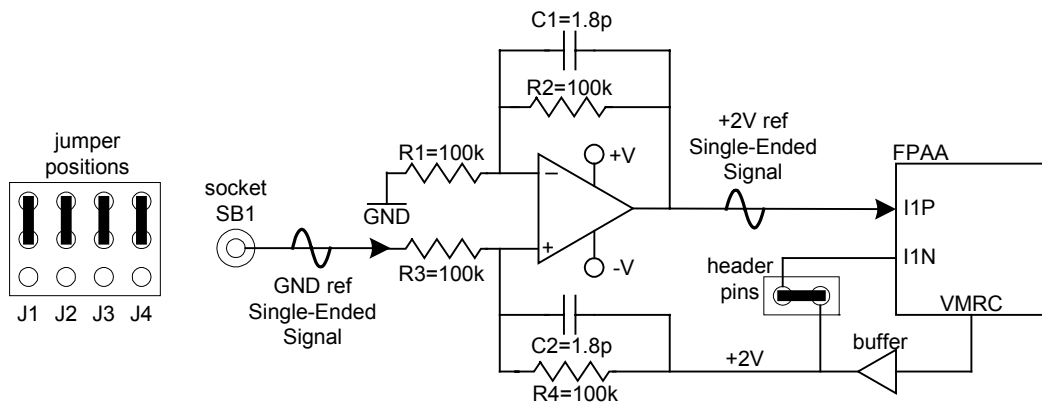


Figure 6: Input Level-Shifter (block #1)

If the jumpers are in the lower position then the block is configured as an output stage (figure 7). This figure shows an analog interface block configured as an output, level shifting the +2V referenced differential output from the FPA to ground and converting it to single-ended. The gain of this circuit can be changed by changing the values of the resistors. The gain is given by the following equation:

$$\text{Gain} = R2 / R1 = R4 / R3 \quad - \quad R3 = R1 \text{ and } R4 = R2$$

Note: The output signal from the circuit cannot exceed the supply voltages to the opamp (V+ and V-). Also the 2 input resistors should not be significantly lower than 100kΩ so as to not overload the FPA outputs.

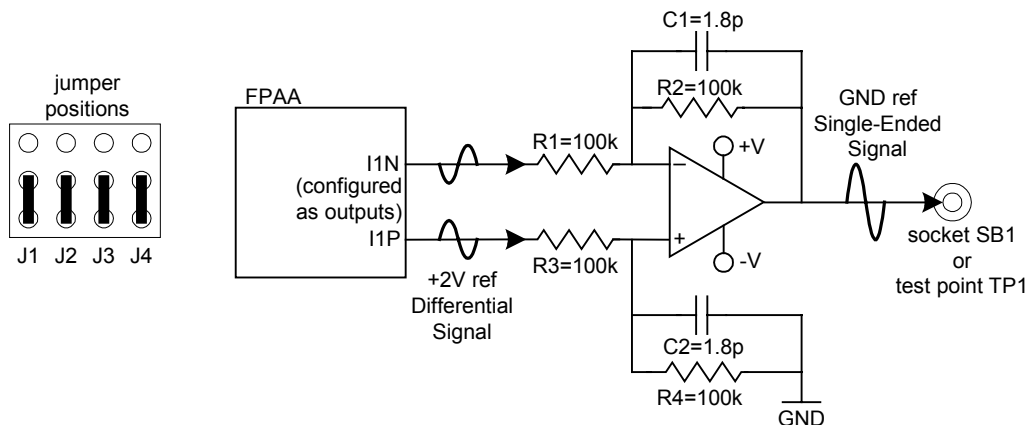


Figure 7: Output Level-Shifter and Diff2Single Converter (block #1)

The analog interface block in figure 5 can also act as a low pass filter – with the corner frequency adjusted by changing the values of the 2 capacitors in figure 5. The default values for the capacitors is 1.8pF and this gives a cut-off frequency at about 1MHz – the response of the default circuit is shown in figure 8. To lower the cut-off frequency you can replace these capacitors with larger ones, the value given by the formula below:

$$C = 1 / (2 * \pi * R * Fc)$$

- Fc is the required cut-off frequency
- C refers to both capacitors (C1 and C2 in block #1)
- R refers to both feedback resistors (R2 and R4 in block #1)

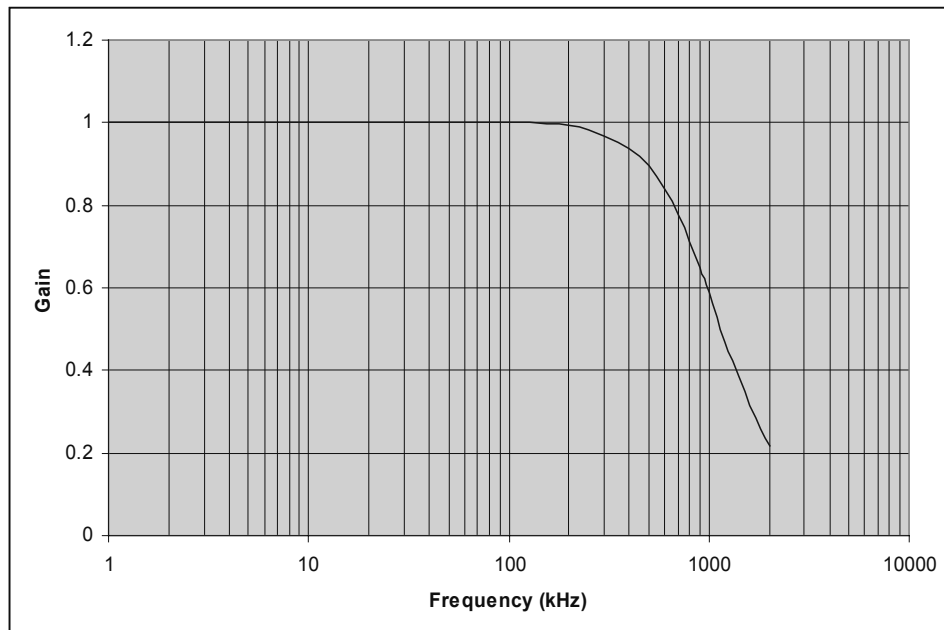


Figure 8: Frequency Response of Analog Interface Block with Default Components

Note: removing the capacitors altogether will not significantly increase the cut-off frequency and will also have the effect of producing a peak in gain of >1 (i.e. a non flat response) close to the cut-off frequency.

Figure 9 shows how to place a single jumper on the block of jumpers (J1-4 in figure 9) in order to connect a socket or test point directly to an FPAA pin. This can be useful for signals that have a floating reference. In such situations it is recommended to connect the other differential input to VMR (buffered) by placing a jumper on the corresponding header pins.

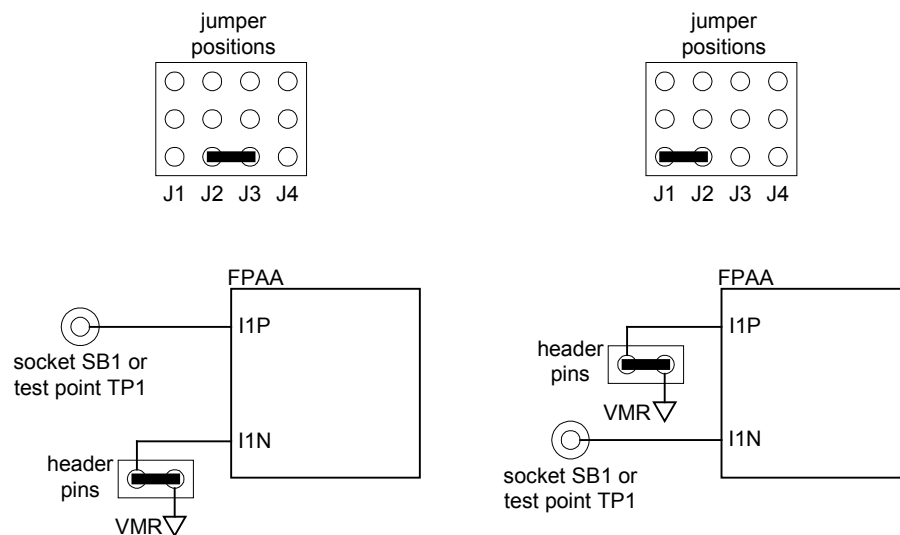


Figure 9: Connecting a Socket Directly to the FPAA (block #1)

Finally, the jumpers can be omitted from the circuit in figure 5 and the user can wire up the opamp as required. As an example, the circuit in figure 10 shows how 2 analog interface blocks have been used to make a single-ended to differential converter and level-shifter circuit. Note how block #2 has been used as a standard input level-shifter (as in figure 6) and 3 wires have been added to block #1 to make it into an inverting level-shifter for input to I2N of the FPAA.

5.0 Evaluating Multi-chip Designs – Daisy Chaining

Use shorting jumpers to daisy chain two or more boards. Figure 11 shows how the daisy jumpers at the edge of the board are wired and figure 12 shows how the jumpers should be placed.

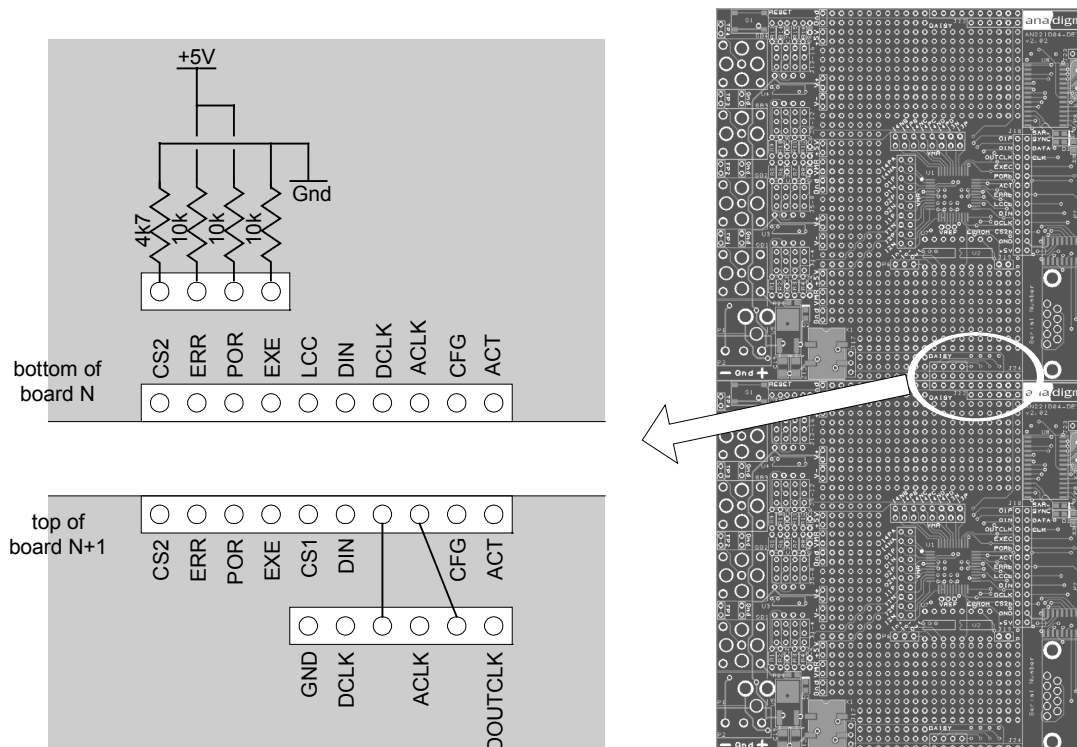


Figure 11: Position and Wiring of Daisy Jumpers

Note 1

When daisy chaining boards, they should be powered in one of the following ways:

- Use a single AC converter into one of the boards and common together the negative, ground and positive posts of the screw terminals of all the boards.
- Use a regulated bench supply into the screw terminals of one of the boards and common together the negative, ground and positive posts of the screw terminals of all the boards.

Note 2

All jumpers should be removed from J17 and J18 on all boards in the chain except the last (the last board is connected to the PC serial port – see figure 13).

Note 3

The pull-ups and pull-downs described in figures 11 and 12 are required for 4 of the FPAA's digital pins. (CS2b, ERRb, PORb and EXECUTE). When chaining boards, only 1 set of pull-ups and pull-downs are required so they must be disconnected on all but one of the boards.

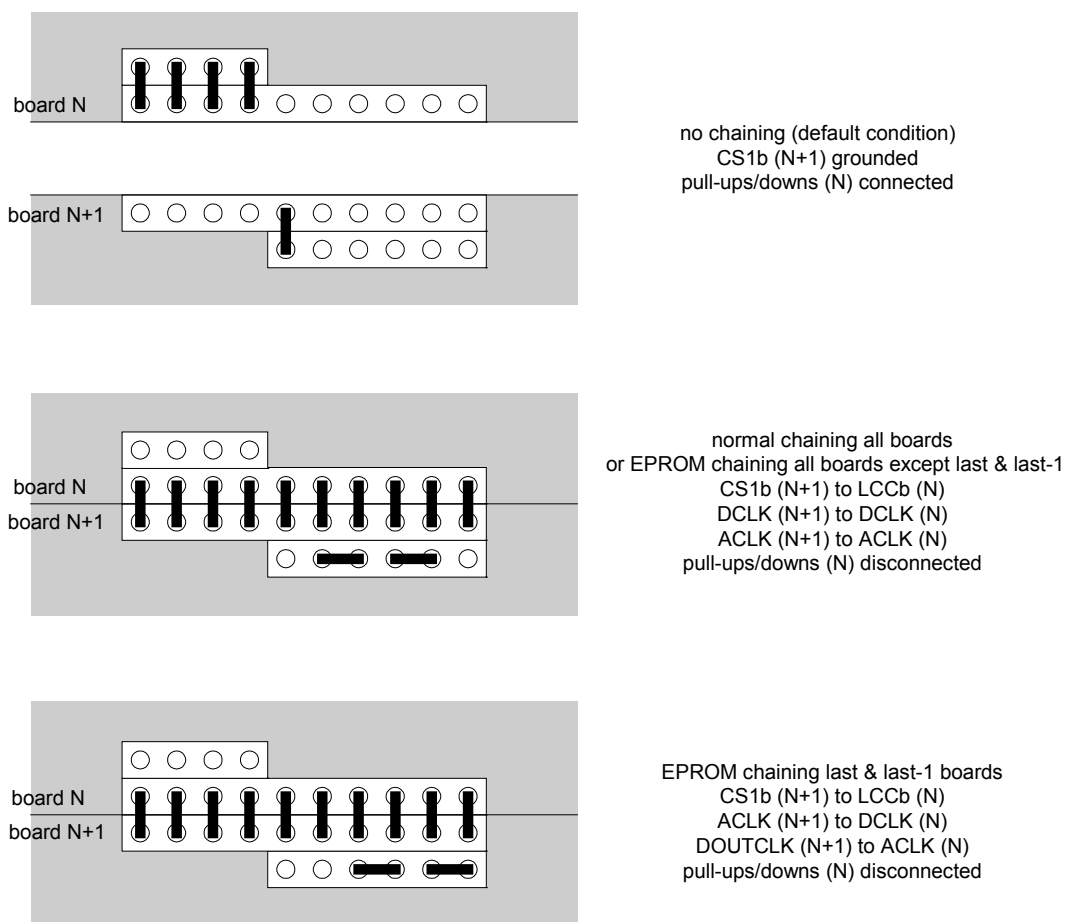


Figure 12: Jumper Settings for Daisy Chaining

Figure 13 shows a system of 3 boards chained together with the correct jumper settings and load order as relating to the AnadigmDesigner® 2 circuit.

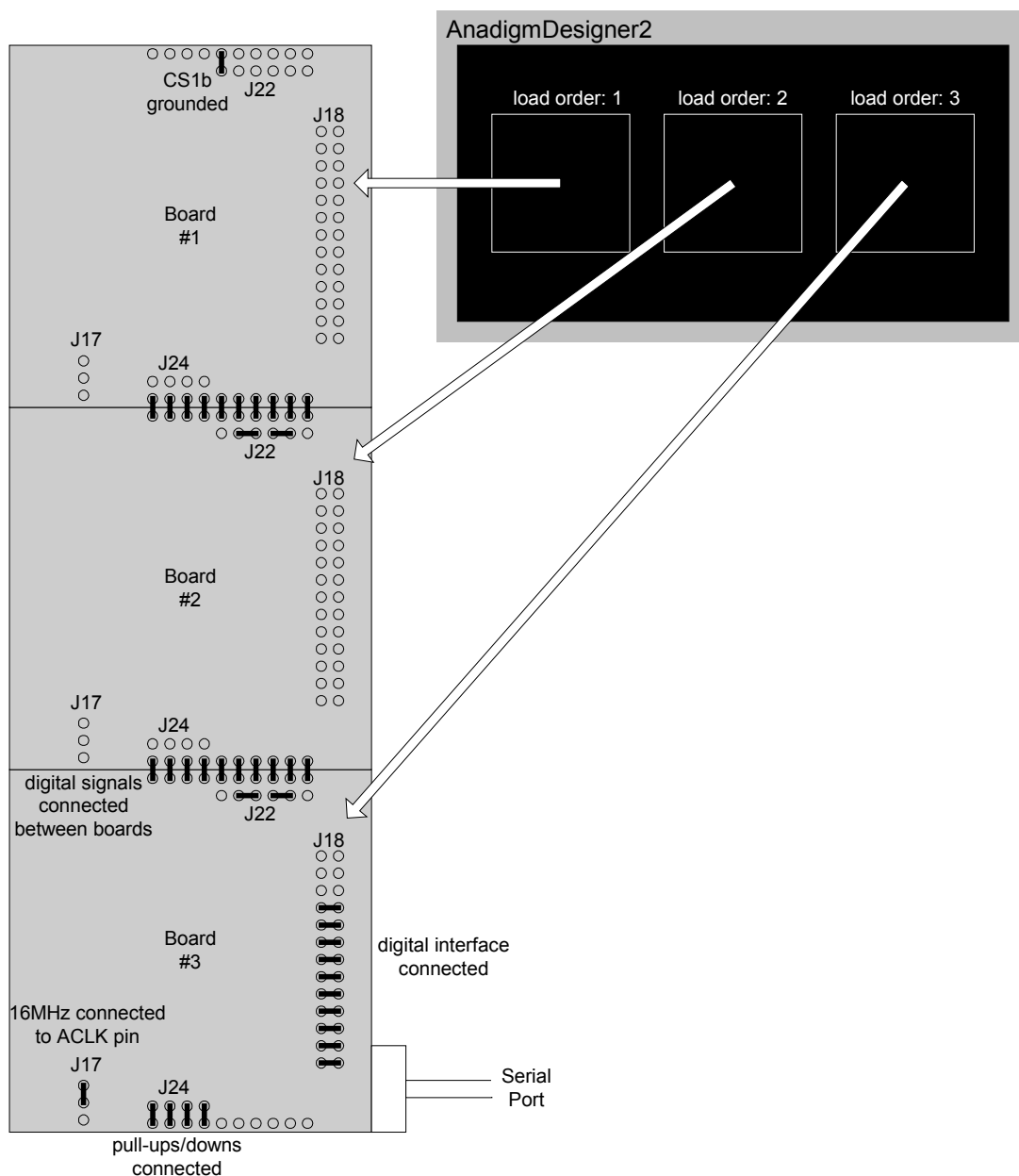


Figure 13: Jumper Settings and Load Order for 3 Chained Boards in Normal Mode

Figure 14 shows another system of 3 boards chained together but this time configured from an EPROM.

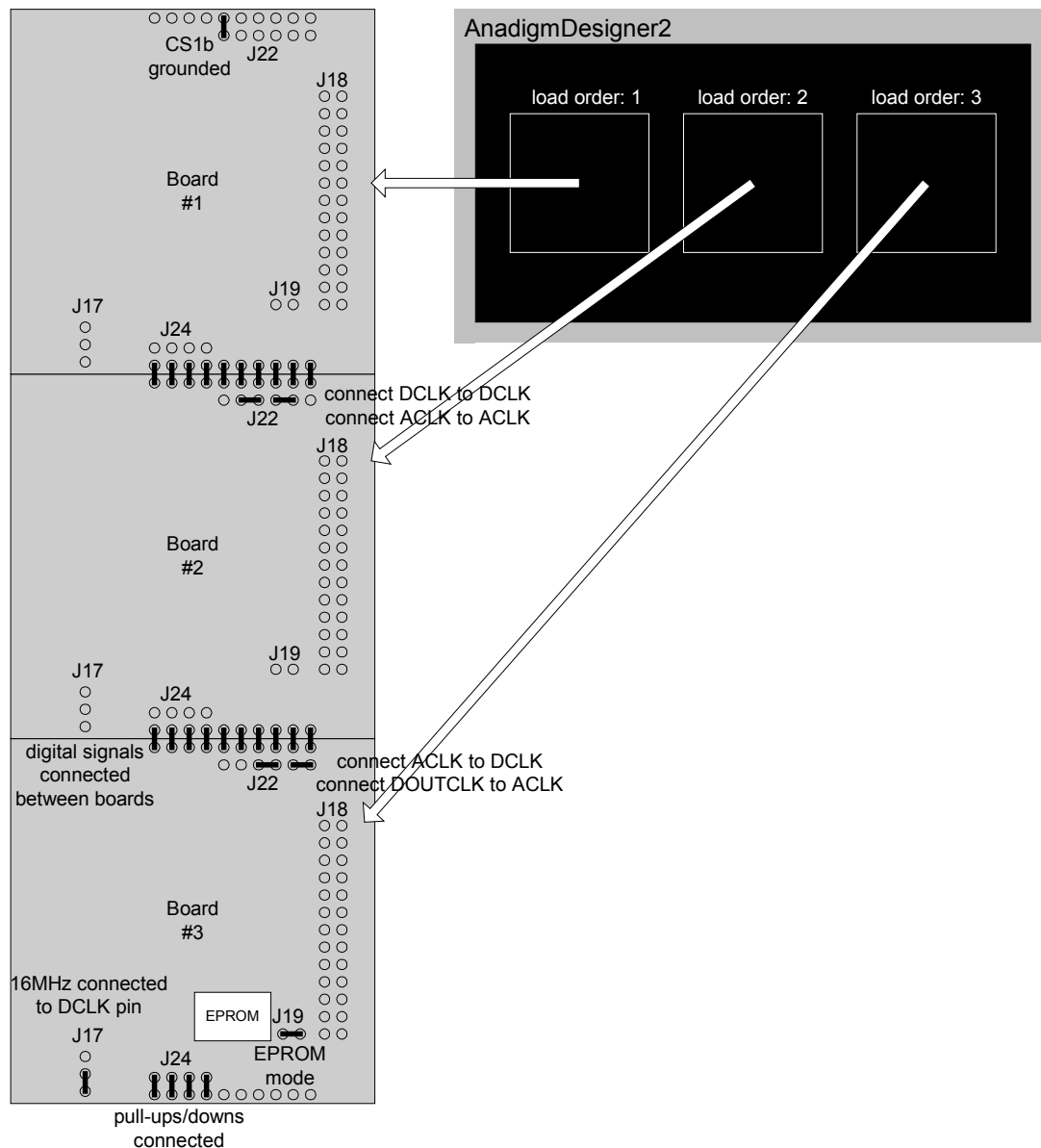


Figure 14: Jumper Settings and Load Order for 3 Chained Boards in EPROM Mode

6.0 Other Features

V_{REF} Pins and Spare Opamp

The 3 reference pins on the FPAA device – VMRC (+2.0V), VREFPC (+3.5V) and VREFMC (+0.5V) – have been brought out to pads.

The VMRC pin has been buffered using an opamp to provide buffered VMR for the whole board. There is also a spare opamp and its pins have been brought out to pads. This opamp can be used to buffer either VREFPC or VREFMC for use in such applications as sensor interfacing, or it can be used for any other custom function. The spare opamp is powered to 0 and +5V only.

Header Pins

All of the analog I/Os of the FPAA are brought out to header pins for easy connection. Next to these header pins is a second row of header pins connected to buffered VMR (+2V). This allows the user to connect any FPAA analog I/O to VMR using shorting jumpers, resistor jumpers or capacitor jumpers.

EPROM

There is an SPI EEPROM socket on the board. To put the board into EPROM mode:

1. Put a jumper onto J19 which sits right next to the EPROM socket, and
2. Pull all of the jumpers from the digital interface J18.

In EPROM mode the 16MHz oscillator module drives the DCLK pin of the FPAA instead of the ACLK pin as normal (when daisy chaining boards, this only applies to the first board in the chain). Putting the jumper J17 in the lower position allows the 16MHz oscillator module to drive the DCLK pin.

Reset Button

There is a reset button in the top left of the board. This resets both the FPAA and the PIC (digital section). In EPROM mode, press the reset button to load the circuit from the EPROM into the FPAA.

Digital Section

The digital section of the evaluation board is provided only so that there is a convenient (serial) interface from the board to a PC to enable direct configuration of the FPAA from AnadigmDesigner^{®2}, normal use of the FPAA does not require this digital interface, the FPAA can be programmed directly from an SPI interface. It is convenient when first developing an analog circuit within the FPAA to have the direct interface to AnadigmDesigner^{®2}, when the circuit(s) are implemented into a final design either a host uP (or DSP) or an EEPROM is normally used to store and configure the FPAA.

The digital section of the board consists of a RS-232 transceiver, a PIC microcontroller (to perform serial ASCII to bit conversion),. It also includes a green LED (to indicate successful configuration), and a red LED (to indicate failed configuration)

The digital section sits along the right side of the board and is connected to the rest of the board by a set of jumpers J18. It is possible to cut away the digital section to leave a purely analog board with header pins on the edge to provide an external digital interface.

If the digital section of the development board is removed or ignored (by pulling jumpers J18), the FPAA can be configured directly using any processor with an SPI interface (or port configured with appropriate signals) by connecting signals directly to the FPAA side of J18. Fully dynamic control of the FPAA's analog circuitry can be realised under software control via this connection.

Note

Anadigm[®] does not recommend any specific processor/controllers – our products work with most processors.

Anadigm[®] recommends that our customers use their own processor development boards and connect via jumper 18 to Anadigm's FPAA for fully dynamic control of the FPAA, in preference to re-engineering the digital section of this development board.

7.0 Jumpers

Table 1 shows a complete list of the jumpers on the board and figure 15 shows their positions.






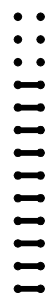




Jumper	Function	Default State	Default Condition
J1-4	Analog Interface Block #1 All 4 in upper position – configured as input i/f All 4 in lower position – configured as output i/f Note: when used as an input i/f there should also be a jumper between the I1N header pin and VMR		Output interface
J5-8	Analog Interface Block #2 All 4 in upper position – configured as input i/f All 4 in lower position – configured as output i/f Note: when used as an input i/f there should also be a jumper between the I2N header pin and VMR		Output interface
J9-12	Analog Interface Block #3 All 4 in upper position – configured as input i/f All 4 in lower position – configured as output i/f Note: when used as an input i/f there should also be a jumper between the I3N header pin and VMR		Input interface Note: also a jumper between I3N header pin and VMR (see figure 6)
J13-16	Analog Interface Block #4 All 4 in upper position – configured as input i/f All 4 in lower position – configured as output i/f Note: when used as an input i/f there should also be a jumper between the I4NA header pin and VMR		Input interface Note: also a jumper between I4NA header pin and VMR (see figure 6)
J17	16MHz Oscillator Module Upper position – ACLK driven by 16MHz Lower position – DCLK driven by 16MHz No jumper – osc module disconnected (not disabled)		16MHz connected to ACLK pin of FPAA
J18	Digital Interface Connects +5V, ground and all digital signals between the analog and digital sections of the board. The top 3 jumpers connect the SAR ADC signals to the PIC		+5V, ground and all digital signals connected between analog and digital sections. The SAR ADC signals are not connected to the PIC in the default state.
J19	EPROM Place a jumper on J19 to use the EPROM Note 1: an EPROM must be placed in the socket next to J19 as it is not provided by default. Note 2: remove all jumpers from J18 when using the EPROM. Note 3: J17 must be placed in the lower position so that the DCLK pin is driven by 16MHz.		Not in EPROM mode
J22	Daisy chaining and CS1b to ground Note: when daisy chaining, CS1b is grounded on the first board only – see figures 10,11		No daisy chaining and CS1b grounded
J23	Programming the PIC (factory use only)		Normal operating mode
J24	Daisy chaining and pull-ups/downs Note: when daisy chaining, the pull-ups/downs are connected on the last board only – see figures 10,11		No daisy chaining and all pull-ups and pull-downs connected

Table 1: Summary of Development Board Jumpers

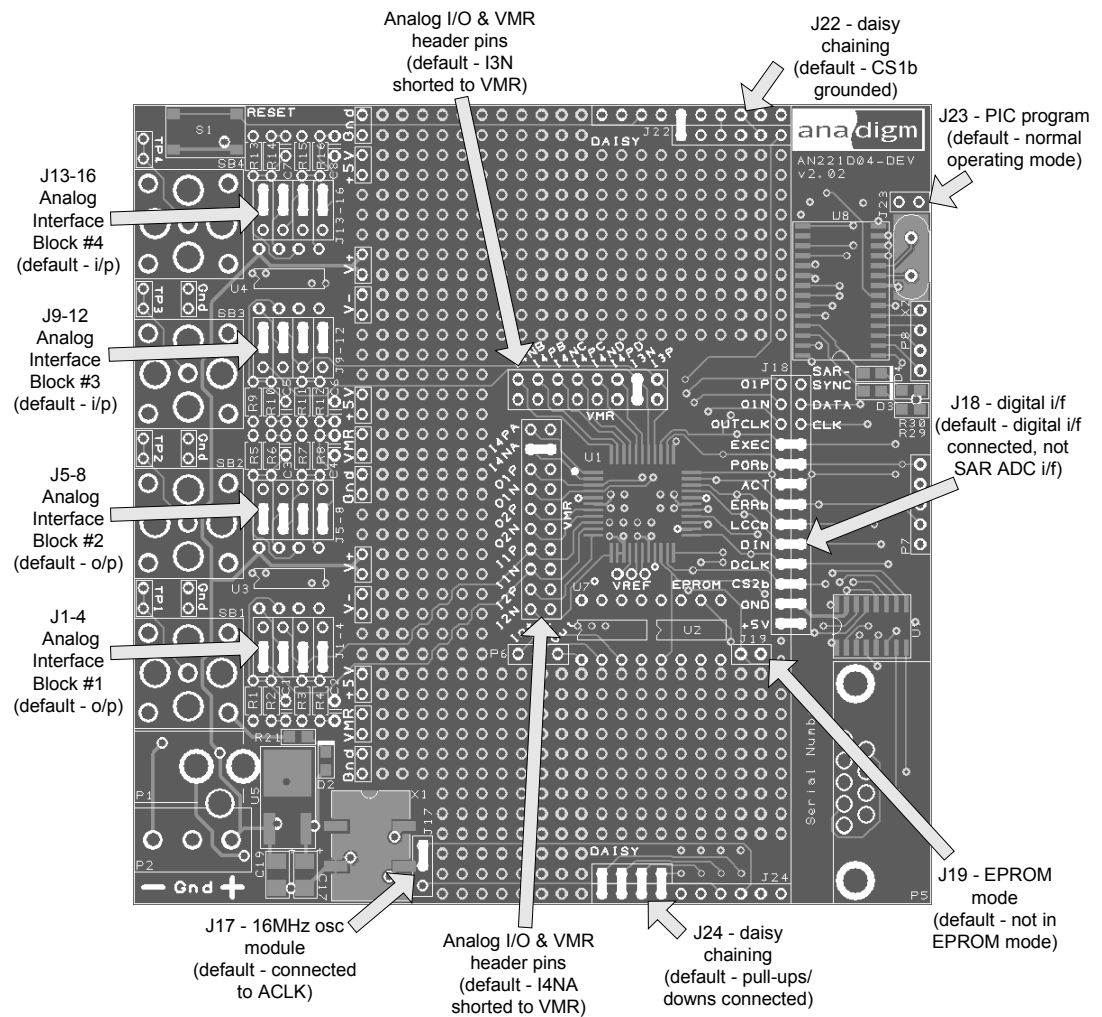


Figure 15: Positions of Jumpers and Default Settings

8.0 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Comment
DC Power Supply 3.5mm jack socket	V_{jack}	10.5	12	20	V	DC voltage only, must be regulated Centre pole is positive, outer sleeve is ground
DC Power Supply screw terminal “+” post	V+	+5.5	+6	+10	V	DC voltage only, must be regulated Voltage is relative to “Gnd” post
DC Power Supply screw terminal “-” post	V-	-10	-6	0	V	DC voltage only, must be regulated Voltage is relative to “Gnd” post
FPAA Input Voltage	F_{in}	-0.5		+5.5	V	Direct input to FPAA on analog IO header pins or digital pins (J18)
FPAA Output Voltage	F_{out}	-0.5		+5.5	V	Direct output from FPAA on analog IO header pins or digital pins (J18)
Analog Interface Block Input Voltage	A_{in}	V-		V+	V	Power supply into screw terminal
Analog Interface Block Input Voltage	A_{in}	-4.75		$V_{\text{jack}} - 5.25$	V	Power supply into jack socket
Analog Interface Block Output Voltage	A_{out}	V-		V+	V	Power supply into screw terminal
Analog Interface Block Output Voltage	A_{out}	-4.75		$V_{\text{jack}} - 5.25$	V	Power supply into jack socket
RS-232 Input Voltage	R_{in}	-30	+/-10	+30	V	Standard RS-232 signal levels
RS-232 Output Voltage	T_{out}	-15	+/-10	+15	V	Standard RS-232 signal levels
Operating Temperature	T_{op}	10		50	°C	Ambient Operating Temperature
Storage Temperature	T_{stg}	-20		70	°C	Ambient Storage Temperature

